REMARKS

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Rejections under 35 U.S.C. §102(e)

With respect to the rejection of claim 4 under 35 U.S.C. §102(b) as being anticipated by Wright (US 6,467,042), Applicant respectfully traverses the rejection at least for the reason that Wright fails describe each and every limitation recited in the rejected claims.

The present invention is directed to an interface circuit provided for each of a first device set as a master side and a second device set as a slave side, for performing a serial data transmission between the first and second devices on the basis of a control signal which is output from the master side. The interface circuit includes a detection portion which monitors the control signal to output a detection signal when there is a change in the control signal, and a process control portion which generates and switches an operation-enable signal and operation disable signal each time the detection signal is supplied thereto.

The interface circuit further includes an oscillation circuit which generates a clock signal for data transmission only when the operation-enable signal is supplied thereto, and a transmission function which performs the serial data transmission on the basis of the clock signal.

According to Applicant's claimed invention, wherein an embodiment is shown in, e.g., Fig. 1 of the application, the oscillation circuit (i.e., oscillation circuit 60) generates a clock signal (i.e., CK) for data transmission only when an operation-enable signal (i.e., ENB) is supplied to the oscillation circuit. Further, the transmission function (i.e., 80) performs serial transmission upon the presence of the clock signal (CK). By generating a clock signal for data transmission only when the operation-enable signal is supplied to the oscillation circuit, power consumption can be advantageously reduced.

In the rejection, the Examiner contends that Wright describes a clock generator (106), in Fig. 2 and column 3, lines 30-35 and column 4, lines 14-19, as being equivalent to Applicant's claimed oscillation circuit. However, Applicant respectfully submits that the clock generator (106) of Wright does not function in similar manner as Applicant's

oscillation circuit, at least because of its interconnection with a processor core 108, Serial Interface Engine (SIE) 110, and suspend/sleep controller 104 of Wright, which in combination perform a completely different function than Applicant's claimed invention.

With respect to column 3, lines 30-35 of Wright, Wright actually states:

> *The clock generator 106 may generate a signal (e.g., CLK) and a signal (e.g., CLK2) that may be used to clock the circuit 100. However, the signal CLK is generally only presented to the processor 108 and the signal CLK2 is generally only presented to the SIE 110. The signals CLK and CLK2 may have the same or different frequency and/or phase.*

Further, column 4, lines 14-19 of Wright actually states:

> *The embodiment of FIG. 3 may insert sleep/suspend states after each packet has been processed without losing any data. If the oscillator 106 wakes up fast enough, the microcontroller 100 may immediately return to the suspend state after every marker, since the device could re-wake-up during subsequent traffic.*

Further, column 3, lines 21-29 and Fig. 2 of Wright describes that the clock generator 106 is made to enter into the sleep/suspend state in response to a control signal (SS) from the sleep/suspend controller 104, which also controls the processor core 108 and the SIE 110. Hence, viewing the clock generator of Wright in proper context, Applicant respectfully asserts that, although Wright describes a clock generator, there is no teaching, disclosure, or suggestion in Wright for an oscillation circuit generating a clock signal for data transmission only when an operation-enable signal is supplied to the oscillation circuit. Further, there is no teaching, disclosure, or suggestion in Wright for a transmission function performing serial transmission upon the presence of the clock signal from the oscillation circuit that receives the operation-enable signal, as recited in Applicant's claim 4.

In contrast with the clock generator of Wright, the oscillation circuit of the presently claimed invention does not enter into the sleep/suspend state nor wake up from a sleep/suspend state after each packet has been processed, as does the clock generator of Wright. In Applicant's invention, the oscillation circuit oscillates simply generates or output a clock signal (CK) for data transmission only when the operation-enable signal (ENB) is supplied thereto.

Applicant respectfully submits that the oscillation circuit of the present invention is configured as a "gated-clock oscillator" wherein the oscillation signal output is gated by the control signal (ENB). Hence, Applicant's oscillation circuit cannot be put in a "sleep/suspend" state in similar manner to that of the clock generator of Wright. Accordingly, in Applicant's claimed invention, a clock signal for data transmission (CK) can be immediately output from the oscillation circuit in response to the control signal (ENB) input, which is completely different from the disclosure of Wright.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in Wright, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claim 4, under 35 U.S.C. §102(a), as anticipated by Wright is improper.

In view of the amendment and arguments set forth above, Applicant respectfully requests the Examiner to consider Wright in its entirety as set forth in MPEP 2141.02(VI). Further, Applicant respectfully requests reconsideration and withdrawal of the §102(a) rejection of independent claim 4.

2. Rejections under 35 U.S.C. §103(a)

With respect to the rejection of claims 5-7 under 35 U.S.C.§103(a) as being unpatentable over Wright, and with respect to the rejection of claims 8 and 9 under 35 U.S.C. §103(a) as being unpatentable over Wright in view of Dehghan (US 6,275,087), Applicant respectfully traverses the rejection at least for the reason set forth above in relation to the §102(a) rejection of independent claim 4, and for the reason that Wright and Dehghan, combined or separately, fail to teach, disclose, or suggest all of the limitation recited in the rejected claims.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

Further, according to MPEP §2141(I), Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case. The Supreme Court in *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966), stated:

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.

Moreover, according to MPEP §2141(II), when applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

> (A) The claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined.

Dehghan generally describes a DC drift canceller circuit. However, similar to Wright, Dehghan fails to teach, disclose, or suggest at least an oscillation circuit which generates a clock signal for data transmission only when the operation-enable signal is supplied thereto, and a transmission function which performs the serial data transmission on the basis of the

clock signal, as recited in independent claim 4 of the present invention. Hence, Wright and Dehghan, combined or separately, fail to teach, disclose, or suggest all of the features in the rejected claims. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the §103(a) rejection of claims 5-9.

3. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 4-9 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Further, while no fees are believed to be due, the Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-4525.

Respectfully submitted,

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